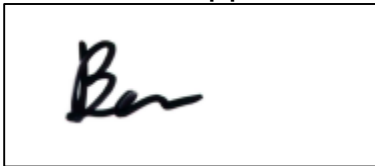


# PRODUCTS SPECIFICATION

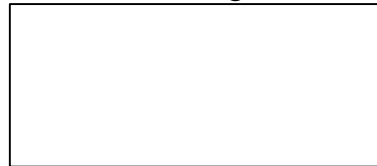
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Description : DVI Connector  
Customer :  
COMOSS P/N : DV Series  
Date of Issue : 20-Sep-2002  
Version : 1.0  
Designer : Ben

Comoss Approved



Customer Signature



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Subject :

Product Specification - DVI connectors.

## 1.0 General

This specification covers the DVI connector including both plug and receptacle for defining its physical, electrical, environmental specification & high frequency characteristics. All performances are designed for complying with DVI (Digital Visual Interface) R 1.0.

## 2.0 Series Description

DV S 23 M 1 0 S 0 0  
(1) (2) (3) (4) (5) (6) (7) (8) (9)

### 1. Series:

DV: DVI Connector

### 2. Types:

S: cable soldering type

E: DIP soldering type

M: SMT type

### 3. Pin count:

17: DVI\_A, (12+5), Analogue

19: DVI\_D, (18+1), Digital, Single link

25: DVI\_D, (24+1), Digital, Dual link

29: DVI\_I, (24+5), Integrate, Dual link

23: DVI\_I, (18+5), Integrate, Single link

### 4. Gender:

M: Male/ Plug

F: Female/ Receptacle

### 5. Contact Finish:

0: Gold Flsah (3u")

1: 15u"

2: 30u"

### 6. Colour of insulator:

0: Black

1: White

2: Grey

### 7. Version:

V: Vertical PCB Mount

S: Straight Cable Soldering

R: Right Angle PCB Mount

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<p><b>8. Mounting option:</b>  0: None for soldering type  1: W/ forklocks only  2: W/ pegs only  3: W/ pegs &amp; forklocks</p> <p><b>9. Locking option:</b>  0: Thru hole  1: W/ #4-40 UNC thread insert  2: W/ #4-40 UNC thread hex screwlock</p> <p>3.0 <u>Application</u></p> <p>(1) Ambient Temperature Range : -25 to +85 °C.</p> <p>4.0 <u>Overall Dimensions</u>  See attachment.</p>				
5.0 <u>Electrical performance</u>				
Item	Description	Test methods and Condition	Requirements	
5-1	Rated Voltage	Any signal pin with respect to the shield	40 Vac (rms).	
5-2	Rated Current	EIA 364-70 55°C, maximum ambient 85°C, maximum temp. change	1.5 Amp min.	
5-3	LLCR (Contact Pairs)	EIA 364-23	Initial: 20mΩ Max. Change: 10mΩ	
5-4	Shell Resistance	EIA 364-06A Contact resistance measured from receptacle shell leg to plug cable braid. Test current =100mA. Test voltage=5Vdc open circuit maximum.	Initial: 50mΩ Maximum change from original: 50mΩ	
5-5	Insulation Resistance	EIA 364-21 Test between adjacent contacts and contacts and shell at test voltage 500Vdc+/- 50Vdc Method C, unmated and unmounted	1GΩ Minimum.	
5-6	Dielectric Withstanding Voltage	EIA 364-20 Test between adjacent contacts. 500Vdc+/-50Vdc, Method C, unmated and unmounted Barometric pressure of 15 psi	No flashover No sparkover No excess leakage No breakdown	

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<b>6.0 Mechanical performance</b>				
Item	Description	Test methods and Condition	Requirements	
6-1	Mating Force	EIA 364-13 Measure force necessary to mate connector at rate of 25mm per minute.	4.5 kgf maximum.	
6-2	Unmating Force	EIA 364-13 Measure force necessary to unmate connector at rate of 25mm per minute.	1 kgf min. 4 kgf max.	
6-3	Durability	EIA 364-09 Automatic cycling to 100 cycles Rate: 100+/-50 cycles/hr	LLCR: max change 10mΩ (All samples to be mated)	
6-4	Vibration	EIA 364-28 Condition III, Method 5A, 15 minutes/axis	No discontinuity at 1us or longer. Test per EIA 364-46	
6-5	Mechanical Shock	EIA 364-27 Condition A	No discontinuity at 1us or longer. Test per EIA 364-46	
<b>7.0 Solderability</b>				
Item	Description	Test methods and Condition	Requirements	
7-1	Solderability	Solder Time : 3 +/- 0.5 Sec. Solder Temperature : 245 +/-5°C	75% minimum.	
7-2	Resistance to soldering Heat	Immerse test sample into molten solder (260+/-5°C) to 1.2mm from the datum line. The dwell time shall be 5 +/- 0.5 Sec. After 30 Sec. (Interval) immerse the sample into solder (260+/- 5°C) for 3 +/- 0.5 Sec.	No Damage.	
<b>8.0 Environmental performance</b>				
Item	Description	Test methods and Condition	Requirements	
8-1	Thermal Shock	EIA 364-32 10cycles (mated) Test condition I	LLCR: max change 10mΩ (All samples to be mated)	
8-2	Temperature Life	EIA 364-17 Condition 4 (105°C) 250 hours, Method A (mated)	LLCR: max change 10mΩ (All samples to be mated)	

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8-3	Humidity Cycle	EIA 364-31 Conditions A & B, Method III nonenergized omit steps 7a and 7b	LLCR: max change 10mΩ (All samples to be mated)	
<b>9.0 High Frequency Characteristic</b>				
Item	Description	Test methods and Condition	Requirements	
9-1	TMDS Signal time domain Impedance	EIA 364-108 draft Risetime=330 ps (10%~90%) S:G ratio per DVI pin designiation Differential Measurement Specimen Environment Impedance=100Ω differential Source-side receptacle connector mounted on a controlled impedance PCB fixture	100 Ω +/- 15%	
9-2	TMDS Signal time domain Crosstalk: FEXT	EIA 364-90 draft Risetime=330 ps (10%~90%) S:G ratio per DVI pin designiation Differential Measurement Specimen Environment Impedance=100Ω differential Source-side receptacle and the load side plug connector are mounted on a controlled impedance PCB fixture (1) Driven pair, and (2) victim pair	5 % maximum	
9-3	TMDS Signal rise time Degradation	EIA 364-102 S:G ratio per DVI pin designiation Differential Measurement Specimen Environment Impedance=100Ω differential Source-side receptacle and the load side plug connector are mounted on a controlled impedance PCB fixture	160 ps maximum (Note: Converted bandwidth using $BW=0.35/t_{rise}$ yields 2.2 GHz)	

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Item	Description	Test methods and Condition	Requirements	
9-4	Analog RGB Coaxial Signal Time Domain Impedance	EIA 364-108 draft Risetime=700 ps (10%~90%) S:G ratio per DVI pin desigation Single-ended Measurement Specimen Environment Impedance=75Ω Single-ended Source-side receptacle connector mounted on a controlled impedance PCB fixture	75 Ω +/- 10%	
9-5	Analog RGB Coaxial Signal Time Domain Crosstalk: FEXT	EIA 364-90 draft Risetime=700 ps (10%~90%) S:G ratio per DVI pin desigation Single-ended Measurement Specimen Environment Impedance=75Ω Single-ended Source-side receptacle conn. is mounted ona controlled impedance PCB fixture and the load side plug connector is terminated to semi-regid coax. (1) Driven line, and (2) victim line	3 % maximum	
9-6	Analog Coaxial Signal Rise Time Degradation	EIA 364-102 S:G ratio per DVI pin desigation Single-ended Measurement Specimen Environment Impedance=75Ω Single-ended Source-side receptacle conn. is mounted ona controlled impedance PCB fixture and the load side plug connector is terminated to semi-regid coax.	140 ps maximum (Note: Converted bandwidth using $BW=0.35/t_{rise}$ yields 2.5 GHz)	